WHAT IS CLAIMED IS:

1. A method of preparing patterned structures on a substrate, comprising:

applying a polymerizable composition to an upper surface of the substrate;

placing an electrically conductive template above the polymerizable composition;

applying an electric field between the electrically conductive template and the substrate, wherein the applied electric field creates an electric static force that attracts a portion of the polymerizable composition toward the template; and

polymerizing the polymerizable composition while the electric field is applied to the electrically conductive template and the substrate,

2. The method of claim 1, wherein the polymerizable composition is an ultraviolet light curable composition.

3. The method of claim 1, wherein the polymerizable composition is an ultraviolet light curable composition, and wherein the UV curable composition is a liquid.

4. The method of claim 1, wherein the electrically conductive template comprises indium tin oxide.

5. The method of claim 1, wherein applying the electric field to the template and the substrate causes a portion of the polymerizable composition to contact a portion of the template.

6. The method of claim 1, wherein the polymerizable composition is attracted to the template but does not contact the template when the electric field is applied to the template and the substrate.

7. The method of claim 1, further comprising etching the polymerized polymerizable composition.

8. A substrate comprising patterned structures made by the method of claim 1.

9. An apparatus for altering a shape of a substrate, comprising:

a holder configured to couple to and support the substrate;

a plurality of pressure application devices coupled to the holder, wherein the pressure application devices are configured to apply a deforming force to the holder such that a shape of the holder is altered during use;

wherein the substrate is coupled to the holder such that the shape of the substrate substantially conforms to the shape of the holder during use.

10. The apparatus of claim 9, wherein the holder comprises a vacuum chuck.

11. The apparatus of claim 9, wherein the pressure application devices comprise piezoelectric actuators.

12. The apparatus of claim 9, further comprising a detector configured to measure the planarity of the substrate during use.

13. The apparatus of claim 9, wherein the substrate comprises a silicon wafer, a GaAs wafer, a SiGeC wafer, or an InP wafer.

14. A method of preparing patterned structures on a substrate, comprising:

applying a polymerizable composition to an upper surface of the substrate;

applying a plurality of forces to the substrate such that the shape of the substrate is altered.

placing an electrically conductive template above the polymerizable composition;

applying an electric field between the electrically conductive template and the substrate, wherein the applied electric field creates an electric static force that attracts a portion of the polymerizable composition toward the template; and

polymerizing the polymerizable composition while the electric field is applied to the electrically conductive template and the substrate.

15. The method of claim 14, wherein the altered substrate exhibits a planarity of less than about 0.25 μm over the entire substrate.

16. A method of making a template for preparing patterned structures on a substrate, comprising:

depositing a layer of an electrically conductive material that is substantially transparent to visible and ultraviolet light on a non-conductive material that is substantially transparent to visible and ultraviolet light;

etching the electrically conductive material to form a pattern of structures that are complimentary to a predetermined pattern of structure to be produced on a substrate.

17. The method of claim 16, wherein the electrically conductive material comprises indium tin oxide.

18. The method of claim 16, wherein the non-conductive material comprises fused silica.

19. The method of claim 16, wherein the pattern of structures comprises structures having the smallest feature size to be less than about 100 nm.